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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,396	02/21/2002	Tadaaki Maeda	03500.016212.	5609

5514 7590 04/29/2005

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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,396	MAEDA, TADAAKI	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7 and 10* is/are rejected.

7)☒ Claim(s) *3-4,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/21/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

• Claims 1-10 are pending for reexamination.

Claim Objections

1. Claims 3-4, 8, 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1, 5-7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakimi U.S. Patent 5,640,357 in view of Sinclair et al U.S. Patent 6,848,058 and Lee U.S. Patent 6,065,124.

4. As per claim 1, Kakimi teaches a memory control device comprising:

a memory controller [52] for outputting a clock enables signal [RAS E9, CAS E10, fig.3];

a power controller [54, 70, fig. 3];

Pull-down resistance [66, 68, fig. 3];

However, Kakimi is silent in teaching a memory controller for directly outputting clock enable signal to DRAM without any intervening switches. Sinclair et al teach another power saving system where clock signals and system controllers are suspended during the sleep mode. Specifically, Sinclair et al teach a memory controller [16 fig. 1] for controlling an operation of a DRAM and for directly outputting a clock enable signal to said DRAM without any intervening switches [col. 2 lines 25-34].

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the Kakimi's memory controller indirect signaling with the directly outputting of a clock enable signal of Sinclair et al, in this way, the clock enable signal functions as a direct control signal for putting the DRAM into the self refresh mode as well as a control signal for releasing the DRAM from the self refresh mode.

Kakimi further teaches, if power controller detects the power stoppage of main power supply during a normal operation [col. 11 lines 54-58, col. 12 lines 63-67], the power controller is configured to switch a power supply for DRAM from main power supply to the battery power supply [col. 9 lines 18-35, col. 12 line 67- col. 13 line 1]; and

the memory controller changes the clock enable signal for the DRAM to the low level to establish the self-refresh mode based upon the power stoppage signal [reset signal E5, col. 11, lines 60-61] from the power controller whereby the low level signal is being maintain by the pull-down resistance for maintaining the self-refresh mode [col. 11, line 60 – 12, line 8, col. 14, lines 29-41] while the power supply thereto is stopped [col. 14, lines 43-47].

However, Kakimi is silent in teaching the power controller is further configured to stop the supply of power to the memory controller. Lee teaches another method for controlling power

management enable a computer system to have minimum power consumption during a sleep mode. Specifically, Lee teaches, after the DRAM is set to the self-refresh mode, the power controller is further configured to stop the supply of power to the memory controller [col. 5 lines 15-34].

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kakimi and Lee since they both directed to the teaching of reducing power consumption in a computer system during the sleep mode. And Lee teaches the power controller is further configured to stop the supply of power to the memory controller to facilitate a simpler and easier method for separating power between the main memory and the memory controller during the sleep mode [col. 6 lines 50-56].

5. As per claim 5, Kakimi teaches wherein power is supplied to memory controller only by main power [fig. 3], and, if main power is stopped, the power is supply to memory controlled until the self-refresh mode of DRAM is established [col. 9 lines 17-51].

6. As per claim 6, George teaches wherein, if power controller detects stoppage of main power, power controller instructs the self-fresh mode by changing an instruction signal for instructing the self-refresh mode to memory controller to active [col. 3 lines 67 to col. 4 lines 1-2].

7. As per claim 7, Kakimi teaches wherein, if power controller detects stoppage of main power, power controller maintains an instruction signal for self-refresh mode [fig. 6A - "backup

inst. Signal"] to active until main power restore and after the instruction signal was made active, system reset is cancel [col. 11 lines 23-35]; and

while the instruction signal is active, the memory controller maintains the clock enable signal [E6, E7, fig. 9] to low level [col. 11 lines 28-32].

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakimi/Usui/Lee in view of George U.S. Patent No. 6,317,657.

8. Kakimi/Usui/Lee is silent in teaching, if the power controller detects the power stoppage of main power supply during the normal operation, the power controller is configured to switch a power supply for the memory controller from the main power supply to the battery power supply. George teaches another system for providing battery back-up of DRAM data upon power failure in which a power down event is detected. Specifically, George teaches, if the power controller detects the power stoppage of main power supply during the normal operation, the power controller is configured to switch a power supply for the memory controller from the main power supply to the battery power supply [SDRAM Power-fig. 1, col. 3 lines 15-26].

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kakimi/Usui/Lee with the method of George since they both directed to the teaching of providing battery back-up of memory data. And George teaches the power controller is configured to switch a power supply for the memory controller from the main power supply to the battery power supply, when power stoppage of main power supply is detected, in order to allow the memory controller the time to establish self-refresh mode of the DRAM in the event the main power is abruptly disconnect. And

After the self-refresh mode of the DRAM is established by memory controller, Lee teaches to stop the supply of power to the memory controller from battery power supply [see discussion in claim 1]

9. Kakimi teaches, if the power controller receivers a power off instruction signal, the power is configured to switch a power supply from DRAM from the main power supply to the battery power supply. However, Kakimi is silent in teaching the power controller monitors voltage of the main power supply. George teaches another system for providing battery back-up of DRAM data upon power failure in which a power down event is detected. Specifically, George teaches the power controller monitors voltage of the main power supply so that, if the voltage is reduced below a predetermined value, the power stoppage is detected [col. 3 lines 14-18]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the power controller of Kakimi with the power controller of George, which capable of monitoring the main power supply, in order to prevent the loss of data in DRAM when the system power is abruptly cut off.

Response to Amendment

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran

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